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METHOD AND APPARATUS FOR AUTOMATIC GAIN CONTROL

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Technical Field

The present invention relates generally to electrical circuits and, more particularly, to techniques for automatic gain control.

Background

Automatic gain control is employed in a variety of applications, for example, to adjust gain as a function of an input signal or other parameters. A typical automatic gain control (AGC) circuit utilizes only analog techniques to control gain, such as for example by varying a bias current or a load resistance. Consequently, these types of AGC circuits are generally limited in their allowable linear dynamic range and/or speed of operation.

A conventional AGC circuit may also employ a peak amplitude detection circuit to sense an output signal amplitude level of the AGC circuit. A drawback of a typical peak amplitude detection circuit is its limited speed of operation, which generally limits the overall speed of operation for the AGC circuit. As a result, there is a need for improved techniques for automatic gain control.

SUMMARY

Systems and methods are disclosed herein to provide automatic gain control. For example, in accordance with an embodiment of the present invention, an automatic gain control (AGC) system is disclosed. The AGC system may employ analog and digital techniques to achieve high-speed AGC having a high linear dynamic range. An overall gain of the AGC system may be controlled through coarse and fine control signals, with the gain monitored via a power detector circuit. Furthermore, the AGC system may be calibrated, for example, to account for process, voltage, and temperature variations.

More specifically, in accordance with one embodiment of the present invention, an automatic gain control system includes an automatic gain control core circuit adapted to apply a gain to an input signal to provide an output signal; a power detector circuit adapted to receive the output signal and provide a first signal which indicates a power level of the output signal; and a processor adapted to control the gain of the automatic gain control core circuit based on the first signal.

In accordance with another embodiment of the present invention, an automatic gain control circuit includes an amplifier adapted to apply a gain to an input signal to provide an output signal; a detector adapted to receive the output signal and provide a first signal based on the output signal; and a processor adapted to provide a coarse gain control signal and a fine gain control signal to the amplifier based on the first signal to control the gain of the amplifier, wherein the processor determines a reference level value for the output signal by providing a calibration signal to the detector and setting the reference level value based on the first signal.

In accordance with another embodiment of the present invention, a method of providing automatic gain control includes providing a gain to an input signal to provide an output signal; monitoring a power level of the output signal; and providing a coarse gain control and a fine gain control to control the gain based on the monitoring to maintain the output signal within a desired signal level range.

In accordance with another embodiment of the present invention, a method of calibrating and monitoring an automatic gain control circuit includes providing a calibration signal whose signal level is estimated to provide a reference value; setting a range for an output signal based on the reference value; providing a gain to an input signal to provide the output signal; monitoring an output signal level of the output signal; and adjusting a coarse gain of the gain to maintain the output signal within the range.

The scope of the invention is defined by the claims, which are incorporated into this section by reference. A more complete understanding of embodiments of the present invention will be afforded to those skilled in the art, as well as a realization of additional advantages thereof, by a consideration of the following detailed description of one or more embodiments. Reference will be made to the appended sheets of drawings that will first be described briefly.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a block diagram illustrating an automatic gain control system in accordance with an embodiment of the present invention.

Fig. 2 shows a flowchart illustrating an exemplary operational flow for the automatic gain control system of Fig. 1 in accordance with an embodiment of the present invention.

Fig. 3 shows a block diagram illustrating an exemplary implementation for a portion of the automatic gain control system of Fig. 1 in accordance with an embodiment of the present invention.

Fig. 4 shows a circuit diagram illustrating an exemplary circuit implementation for a portion of the block diagram of Fig. 3 in accordance with an embodiment of the present invention.

Figs. 5a through 5g show circuit diagrams illustrating exemplary implementations for a portion of the circuit diagram of Fig. 4 in accordance with an embodiment of the present invention.

Fig. 6 shows a block diagram illustrating an exemplary implementation for a portion of the automatic gain control system of Fig. 1 in accordance with an embodiment of the present invention.

Fig. 7 shows a circuit diagram illustrating an exemplary circuit implementation for a portion of the block diagram of Fig. 6 in accordance with an embodiment of the present invention.

Embodiments of the present invention and their advantages are best understood by referring to the detailed description

that follows. It should be appreciated that like reference numerals are used to identify like elements illustrated in one or more of the figures.

DETAILED DESCRIPTION

Fig. 1 shows a block diagram illustrating an automatic gain control system 100 in accordance with an embodiment of the present invention. System 100 may be viewed as a mixed signal system, which utilizes analog and digital signals to perform its intended function of automatic gain control. System 100 includes an automatic gain control (AGC) core 102, a processor 104, an analog-to-digital converter (ADC) 106, a power detector (PD) 108, a digital-to-analog converter (DAC) 110, and switches 120 and 122 (labeled S1 and S2, respectively).

AGC core 102 provides a gain (i.e., amplifies or attenuates) to an input signal 112 (e.g., an analog signal) to provide an output signal 118 (e.g., an analog signal), which is an amplified or attenuated version of input signal 112. Input signal 112 and output signal 118 may represent, for example, a signal having a variable amplitude and a signal having an approximately fixed (desired) amplitude, respectively. PD 108 senses an average power level of output signal 118 when switch 120 is closed and switch 122 is open and is utilized for calibration purposes of system 100 when switch 120 is open and switch 122 is closed. ADC 106 converts a signal received from PD 108 and provides the converted signal to processor 104.

Alternatively, in accordance with an embodiment of the present invention, a conventional peak detector circuit may be substituted for PD 108. Consequently, rather than measure an average power level, a peak amplitude of output signal 118 is

determined and utilized in a similar fashion as is explained herein for a power level indication from PD 108.

Processor 104 (e.g., a microprocessor) monitors and controls certain functions of system 100. Processor 104 controls switches 120 and 122 (e.g., transistors) to place system 100 in the desired mode, a calibration mode and a continuous AGC mode, as explained further herein. Processor 104 also receives the converted signal from ADC 106 and provides control signals 114 and 116 (fine and coarse gain control, respectively) to adjust a gain of AGC core 102. Processor 104 further provides a signal 124 to DAC 110 during the calibration mode to calibrate PD 108.

Processor 104 may place system 100 into the calibration mode (i.e., self-calibration mode) by closing switch 122 and opening switch 120 or into the continuous AGC mode by opening switch 122 and closing switch 120. In the calibration mode, processor 104 calibrates PD 108 by providing a selected digital word (e.g., corresponding to the desired reference level of output signal 118) via signal 124 to DAC 110, which provides an analog equivalent of signal 124 to PD 108. PD 108 provides its output signal to ADC 106, which provides the converted signal to processor 104.

The converted signal from ADC 106, in the calibration mode, represents a reference level value (referred to herein as "ref") of the output signal from PD 108 corresponding to the selected digital word provided by processor 104. Processor 104 may then store the reference level value (ref) and compute desired boundaries (referred to herein as "refmin" and "refmax") around the reference level value (ref) to be utilized during the continuous AGC mode.

Processor 104 transitions from the calibration mode to the continuous AGC mode by opening switch 122 and closing switch 120. In the continuous AGC mode, PD 108 continuously monitors output signal 118 and provides its information to processor 104 via ADC 106. Processor 104 adjusts a gain of AGC core 102 to maintain output signal 118 within a desired signal level range (e.g., power level between refmin and refmax).

As an example, Fig. 2 shows a flowchart 200 illustrating an exemplary operational flow for the continuous AGC mode of system 100 in accordance with an embodiment of the present invention. Processor 104 reads a value (PDout) provided by PD 108 via ADC 106 (step 202) and increases a coarse gain of AGC core 102 (step 206) via control signal 116 (coarse gain control) if the value (PDout) is not greater than or equal to a determined lower boundary (refmin) for output signal 118 (step 204) or decreases a coarse gain of AGC core 102 (step 210) via control signal 116 if the value (PDout) is not less than or equal to a determined upper boundary (refmax) at step 208.

If the value (PDout) is within the desired boundaries, then processor 104 sets a fine gain of AGC core 102 (step 212) via control signal 114 (fine gain control), such as for example to minimize the absolute power of output signal 118 (i.e., to minimize abs|PDout-ref|). Processor 104 reads another value (PDout) provided by PD 108 via ADC 106 (step 214) and increases a coarse gain of AGC core 102 (step 206) if the value (PDout) is not greater than or equal to the lower boundary (refmin) at step 216 or decreases a coarse gain of AGC core 102 (step 210) if the value (PDout) is not less than or equal to the upper boundary (refmax) at step 218. Processor 104 continues to fine tune a coarse gain and a fine gain of AGC core 102 as required to maintain output signal 118 within a desired range.

System 100, in accordance with an embodiment of the present invention, utilizes analog and digital techniques to achieve high-speed automatic gain control for an input signal having a high linear dynamic range. For example, system 100 may provide a linear analog output signal of a desired signal level from an analog input signal having a high dynamic amplitude range. The desired signal level which the output signal will settle to may be auto-calibrated to account for process, voltage, and temperature variations.

System 100 may be designed to monitor (e.g., at a multi-gigahertz rate) output signal 118 of AGC core 102. For example, Fig. 3 shows a block diagram of an AGC core 300 illustrating an exemplary implementation for AGC core 102 of Fig. 1 in accordance with an embodiment of the present invention. AGC core 300 includes a number of gain stages 302 (e.g., g_1, g_2, ..., g_n, where "n" represents the number of desired gain stages 302), with the number of gain stages 302 depending upon the desired overall gain or the gain requirement of AGC core 300.

Each gain stage 302 receives control signals 114 and 116 (e.g., a p-bit fine control bus signal and an m-bit coarse control bus signal, respectively, where "p" and "m" are the desired number of bits to provide the desired degree of control) to provide fine and coarse gain control within the particular gain stage. Thus, the overall gain of AGC core 300 may be divided among gain stages 302(1) through 302(n) (i.e., each gain stage 302, such as gain stage 302(2), may contribute a portion of the overall gain) to obtain a quasi-distributed circuit structure, which may help in maximizing bandwidth. AGC core 300 may also include a direct current (DC) offset correction 304, which provides feedback from output signal 118 to an output terminal of an intermediate gain stage (e.g., an output terminal of gain stage 302(2)) to adjust (e.g., minimize) a DC offset value of output signal 118.

Fig. 4 shows a circuit 400 illustrating an exemplary circuit implementation for one of gain stages 302 (e.g., gain stage 302(1)) of Fig. 3 in accordance with an embodiment of the present invention. Circuit 400 includes a number of digitally-switched transconductance (g_m) stages 402 (e.g., stages 402(1), 402(2), ..., 402(m), where "m" corresponds to the number of desired stages and also the number of bits required from control signal 116 for coarse gain control).

Each stage 402 includes a pair of switches 410 (e.g., switches 410(1a) and 410(1b), 410(2a) and 410(2b), through 410(ma) and 410(mb) corresponding to stage 402(1), stage 402(2), through stage 402(m), respectively) which provide coarse control gain for circuit 400. Control signal 116, which includes "m" bits or bits g_{m1} through g_{mm}, provides coarse gain control by controlling switches 410 (e.g., g_m switches) within circuit 400.

For example, if a first bit (g_{m1}) of control signal 116, corresponding to stage 402, is asserted, then switch 410(1a) is closed and switch 410(1b) is opened so that stage 402(1) provides its gain to input signal 112. If the first bit (g_{m1}) of control signal 116 is deasserted, then switch 410(1a) is opened and switch 410(1b) is closed so that stage 402(1) does not provide its gain to input signal 112. Similarly, a second bit (g_{m2}) through to the last bit (m-bit or g_{mm}) of control signal 116 controls corresponding switches 410(2a, 2b) to 410(ma, mb) of corresponding stages 402(2) to 402(m) to provide the desired coarse gain for an output signal 406. Output signal 406 may represent output signal 118 or, if it exists, the following circuit 400 (e.g., the next gain stage 302).

Control signal 114 (fine gain control) controls a current source 408 (e.g., a digitally-controlled current source) to control a bias current provided (e.g., mirrored) for each stage 402 to provide fine gain control to circuit 400. The

combination of coarse and fine gain control enables precise gain control to maintain an approximately constant gain linearity across a wide dynamic range for input signal 112.

Circuit 400 also includes load impedances 404, which may be optimized through appropriate broad-banding techniques to further enhance the bandwidth. As an example, Figs. 5a through 5g show corresponding circuits illustrating exemplary implementations for load impedance 404 of Fig. 4 in accordance with an embodiment of the present invention. For example, Fig. 5a illustrates a shunt (or shunt-peaked) load configuration for load impedance 404 having a resistor (R) in series with an inductor (L). Also shown in Fig. 5a and the following Figs. 5b through 5g are the coupling relationships of output signal 406 relative to the exemplary implementations of load impedance 404 and also relative to a portion of stage 402 showing a transistor of stage 402 receiving input signal 112.

Figs. 5b and 5c illustrate a shunt-series and a series-shunt load configuration, respectively, for load impedance 404 having inductors (L_1 and L_2) coupled to resistor (R) as shown. Fig. 5d illustrates a series-shunt-series load configuration for load impedance 404 having inductors (L_1, L_2, and L_3) coupled to resistor (R) as shown. Figs. 5e and 5f illustrate a T-coil and a T-coil with cross-coupled capacitor (C) load configuration, respectively, for load impedance 404 having inductors (L_1 and L_2) with associated magnetic coupling factor (K). Fig. 5g illustrates a series-T-coil load configuration for load impedance 404 having resistor (R), cross-coupled capacitor (C), inductor (L_3), and inductors (L_1 and L_2) with associated magnetic coupling factor (K).

In general, different types of broad-banding loads can be utilized for bandwidth extension per design requirements or desired application. The transconductance stages 402 (i.e.,

transconductance cell) in combination with broad-band loads enables wide linear dynamic range with high bandwidth (e.g., multi-gigahertz). Further details regarding transconductance cells, including exemplary implementations suitable for each gain stage 302, may be found in U.S. Patent Application No. [unknown, attorney docket no. M-15292 US] entitled "Digitally Controlled Transconductance Cell" and filed November 26, 2003 , which is incorporated herein by reference in its entirety.

Fig. 6 shows a block diagram of a power detector 600, which is an exemplary implementation for PD 108 of Fig. 1 in accordance with an embodiment of the present invention. Power detector 600 includes a correlator 604 followed by a low pass filter 606 to receive an input signal 602 (e.g., from AGC core 102 or DAC 110) and provide an output signal 608 (e.g., to ADC 106). Power detector 600 senses an average power signal level of input signal 602.

Fig. 7 shows a circuit 700 illustrating an exemplary circuit implementation for correlator 604 of Fig. 6 in accordance with an embodiment of the present invention. Circuit 700 is a high-speed correlator (sometimes referred to as a Gilbert cell multiplier). Thus, PD 108 of Fig. 1 may be constructed with a high-speed correlator cell whose speed of operation may be significantly greater than conventional techniques (e.g., peak amplitude detection circuits).

In accordance with one or more embodiments of the present invention, systems and methods are disclosed for providing automatic gain control. For example, utilizing one or more of the techniques disclosed herein, ultra-wide linear dynamic range automatic gain control may be achieved at a high speed (e.g., 10 GHz) of operation. In accordance with one embodiment, a power-detect circuit is employed in an AGC circuit rather than a peak amplitude detect circuit found in conventional devices.

Furthermore, the AGC circuit may be employed as a mixed-signal architecture as opposed to an entirely analog approach. For example, the AGC circuit may utilize gain stages that have digitally-switched transconductance cells. Overall, by utilizing one or more of the techniques discussed herein, a broadband (e.g., multi-gigahertz bandwidth) AGC circuit may be designed having a reduced input sensitivity level and/or higher speed of operation than typical AGC circuits.

Embodiments described above illustrate but do not limit the invention. It should also be understood that numerous modifications and variations are possible in accordance with the principles of the present invention. Accordingly, the scope of the invention is defined only by the following claims.